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NEW LOWER BOUND TECHNIQUES FOR VLSI

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Abstract: In this paper, we use crossing number and wire area arguments to find lower bounds on the layout area and maximum edge length of a variety of new and computationally useful networks. In particular, we describe

1) an N-node planar graph which has layout area $\Theta(N\log N)$ and maximum edge length $\Theta(N^{1/2}/\log^{1/2}N)$,
2) an N-node graph with an $O(x^{1/2})$-separator which has layout area $\Theta(N\log^2 N)$ and maximum edge length $\Theta(N^{1/2}\log N/\log\log N)$, and
3) an N-node graph with an $O(x^{1-1/r})$-separator which has maximum edge length $\Theta(N^{1-1/r})$ for any $r \geq 3$.

Key Words: area-efficient chip layouts, bisection width, crossing number, graph embedding, mesh of trees, parallel computation, separator, Thompson grid model, tree of meshes, Very Large Scale Integration (VLSI), wire area, wire length

This research was supported by a Bantrell Fellowship and by Defense Advanced Projects Research Agency grant N00014-80-C-0622.

1. Introduction

Recent advances in Very Large Scale Integration (VLSI) circuit technology have made it possible to wire tens of thousands of transistors onto a single chip. In the near fututre, it is expected that fabrication of chips containing *millions* of transistors will be commonplace [MC80]. In order that this massive computational resource be effectively utilized, theoretical researchers have been actively trying to develop models and methods for designing VLSI chips. Most of these efforts have been directed towards producing network layouts which minimize the amount of *area* consumed by the chip. This is due to the fact that small chips are usually much cheaper and more reliable than large chips.

Of the several mathematical models that have been proposed for VLSI computation, the simplest and most widely accepted is the *Thompson grid model* [T79, T80]. The grid model of a VLSI chip is quite simple. The chip is presumed to consist of a grid of horizontal and vertical *tracks* which are spaced apart by unit intervals. The nodes of the network are viewed as points and are located only at the intersection of grid tracks. Wires are routed through the tracks in order to connect pairs of nodes. Although a wire in a horizontal track is allowed to cross a wire in a vertical track (without making an electrical connection), pairs of wires are not allowed to overlap for any distance or to overlap at corners (i.e., they cannot overlap in the same track). Further, wires are not allowed to overlap nodes to which they are not linked. (The routing of wires in this fashion is also known as *layer per direction routing* and *Manhattan routing*.)

The *area of a layout* in the grid model is defined to be the product of the number of horizontal tracks and the number of vertical tracks which contain a node or wire segment of the layout. For example, the layout shown in Figure 1 has area 15.

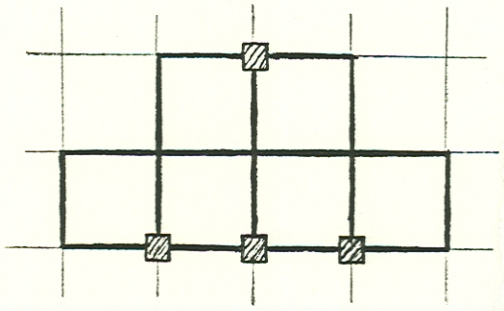

Figure 1: *A layout which has area 15.*

It is easy to construct a layout for the graph shown in Figure 1 which has area 9, implying that the layout in Figure 1 is not optimal. In general, however, it is very difficult to tell if a layout is optimal or even close to optimal. This is due to the fact that relatively little is known about proving *lower* bounds on the area needed to lay out a graph. Past research in this area has centered on the related problem of finding good lower bounds on the bisection width of a graph [T79, T80, V80, LS81]. (The *bisection width* of a graph is the minimum number of edges which must be removed in order to partition the graph into two nearly-equal-sized subgraphs.)

The relationship between bisection width and layout area was first noticed by Thompson [T79] who showed that the layout area of a graph with bisection width B is at least $\Omega(B^2)$. Since that time, Thompson [T80], Vuillemin [V80] and Lipton and Sedgewick [LS81] have all shown how to use information theoretic arguments in order to find good lower bounds on the bisection width of a graph and thus on its layout area. While these methods are useful in finding good lower bounds on the layout area of some networks (such as the shuffle-exchange graph), they have not been of use in resolving two of the key open questions in VLSI theory; namely,

1) "How much area is needed to lay out a planar graph?," and
2) "How much area is required to lay out a graph with an $O(x^{1/2})$-separator?." (An N-node graph is said to have an $f(x)$-*separator* if it can be partitioned into two nearly-equal-sized subgraphs G_1 and G_2 such that at most $f(N)$ edges link G_1 to G_2 and both G_1 and G_2 have $f(x)$-separators.)

The planar graph question is particularly important since (as we will show in Theorem 2) the layout problem for an arbitrary graph can be reduced to that for a planar graph. Although no nontrivial lower bounds are known for either problem, progress has been made on the corresponding upper bounds. In particular, Leiserson [L80a] and Valiant [V81] have shown how to lay out any N-node graph which has an $O(x^{1/2})$-separator in at most $O(N\log^2 N)$ area. As Lipton and Tarjan [LT80] have proved an $O(x^{1/2})$-separator theorem for the class of planar graphs, their $O(N\log^2 N)$ area layout technique also works for planar graphs. Although it is suspected that better layout techniques exist for planar graphs, none have yet been found.

In this paper, we pursue an entirely different strategy in developing new lower bound techniques for VLSI. Whereas previous researchers have been concerned primarily with the bisection width of a network, we shall be concerned with its crossing number and wire area. The *crossing number* of a graph is the minimum

number of pairs of edges which must cross in any planar drawing of the graph. The *wire area* of a graph is the minimum amount of wire which is needed to lay out the graph in the Thompson grid model [T79, T80]. Clearly, the crossing number and wire area are lower bounds on the layout area of any graph. In fact, we will show in Theorem 1 that

$$\Omega(B^2) \leq C+N \leq W \leq A$$

for any N-node graph with bisection width B, crossing number C, wire area W and layout area A.

The preceding inequality implies that every lower bound technique for bisection width can be translated into a lower bound technique for crossing number and wire area. Thus nothing is lost by forgetting about bisection width and concentrating ones efforts on finding good lower bounds for the crossing number and wire area of a graph. In fact, much can be gained. For example, we will use such techniques in this paper to construct

1) an N-node planar graph which has layout area $\Theta(N\log N)$ and
2) an N-node (nonplanar) graph with an $O(x^{1/2})$-separator which has layout area $\Theta(N\log^2 N)$.

The first result demonstrates that not all planar graphs can be laid out in linear area, thus disproving a popular conjecture. The second result indicates that Leiserson and Valiant's $O(N\log^2 N)$-area layout technique for graphs with $O(x^{1/2})$-separators is optimal at least some of the time and thus cannot, in general, be improved.

There has also been a great deal of interest lately in the problem of determining the length of the longest wire in any layout of a network on a chip [BL81, CM81, PRS81]. Bhatt and Leiserson [BL81], in particular, have found some nice upper bounds for this problem. Very little has been accomplished in the way of lower bounds, however, since bisection width arguments do not seem to be applicable to edge length considerations. Crossing number and wire area arguments, on the other hand, *are* very helpful in proving good lower bounds on maximum edge length. In this paper, we will use such arguments to find

1) an N-node planar graph for which any layout must have a wire of length $\Theta(N^{1/2}/\log^{1/2} N)$,

2) an N-node (nonplanar) graph with an $O(x^{1/2})$-separator for which any layout must have a wire of length $\Theta(N^{1/2}logN/loglogN)$ and

3) an N-node graph with an $O(x^{1-1/r})$-separator for which any layout must have a wire of length $\Theta(N^{1-1/r})$ for any $r \geq 3$.

The latter two results achieve the known upper bounds for maximum wire length. They also indicate that some wires in layouts of certain graphs must be very long (possibly as long as the length of the entire layout).

For easy reference, we have summarized our new lower bounds along with the previously known upper and lower bounds in the Tables 1 and 2. The nontrivial upper bounds in Table 1 are due to Leiserson [L80a] and Valiant [V81] while those in Table 2 are due to Bhatt and Leiserson [BL81]. The previously known lower bounds are, for the most part, trivial. The only exception is the $N^{2\alpha}$ area lower bound in Table 1 which is due to Thompson [T80]. In each table, the upper bounds apply to *all* graphs while the lower bounds pertain only to a *special* class of graphs. (For convenience, we have left out the $O(\ )$ notation on the upper bounds and the $\Omega(\ )$ notation on the lower bounds.)

Table 1

Area Bounds

separator	previous lower bound	our lower bound	upper bound
x^{α}, $\alpha < 1/2$	N		N
x^{α}, $\alpha = 1/2$	N	$Nlog^2N$	$Nlog^2N$
x^{α}, $\alpha > 1/2$	$N^{2\alpha}$		$N^{2\alpha}$
(planar)	N	$NlogN$	$Nlog^2N$

Table 2

Maximum Edge Length Bounds

separator	previous lower bound	our lower bound	upper bound
x^α, $\alpha < 1/2$	$N^{1/2}/logN$		$N^{1/2}/logN$
x^α, $\alpha = 1/2$	$N^{1/2}/logN$	$N^{1/2}logN/loglogN$	$N^{1/2}logN/loglogN$
x^α, $\alpha > 1/2$	$N^\alpha/logN$	N^α	N^α
(planar)	$N^{1/2}/logN$	$N^{1/2}/log^{1/2}N$	$N^{1/2}logN/loglogN$

The remainder of the paper is organized as follows. In section 2, we describe the networks for which we will later prove lower bounds. As these networks are new and interesting in their own right (they include new networks for fast sorting and matrix multiplication), we devote a fair amount of space to each. In section 3, we describe the general relationship between crossing number and layout area. We also prove crossing number and maximum edge crossing lower bounds for the nonplanar networks described in section 2. In section 4, we generalize the methods developed in section 3 and prove wire area and maximum edge length lower bounds for a variety of networks. We conclude in section 5 with several remarks, related results and open questions.

Throughout, we limit our discussion of graphs to those with bounded node degree and of layouts to those in the Thompson grid model. Neither constraint is crucial to our results, however. For example, all of the lower bound proofs work equally well for the Lipton-Sedgewick [LS81] (or any similar) model of chip design.

2. Network Constructions

(2a) The 2-dimensional Mesh of Trees

The *2-dimensional nxn mesh of trees* $M_{2,n}$ is defined when n is a power of 2 as follows. Starting with an nxn matrix of nodes and adding nodes wherever necessary,

construct a complete binary tree in each row and column of the matrix. The trees should be constructed so that

1) the leaves in each tree are precisely the nodes in the corresponding row or column of the original matrix, and
2) the subgraph induced on the nodes in each quadrant is $M_{2,n/2}$.

For example, we have drawn $M_{2,4}$ in Figure 2. The nodes in the original *4x4* matrix are represented by dots. The nodes which were added in order to form row trees are drawn as small triangles while those added to form column trees are shown as small squares. Solid lines indicate row tree edges while dashed lines indicate column tree edges.

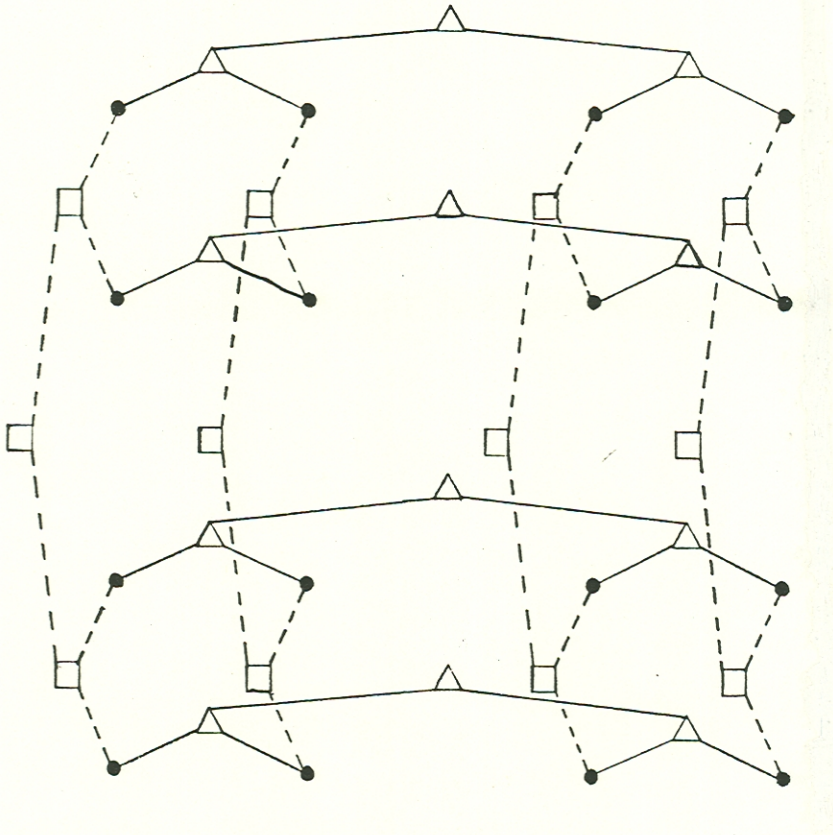

Figure 2: *The 4x4 mesh of trees* $M_{2,4}$.

Notice that if we were to remove the roots of the row and column trees of $M_{2,4}$ and the edges incident to them, we would be left with *4* copies of $M_{2,2}$, one in each quadrant. In general, if we were to remove the nodes and edges in the top k levels

of the binary trees in $M_{2,n}$, we would be left with 2^{2k} copies of $M_{2,n2^{-k}}$. This important property of meshes of trees is used extensively in the proofs of Theorems 3, 4, 5 and 8.

Computationally, the *nxn* mesh of trees is a very powerful network. Among other things, it can be used to

1) multiply a fixed *nxn* matrix by *m* different *n*-vectors in *m+2logn* (word) steps,
2) sort a list of *n* *m*-bit words in *2m+5logn* (bit) steps, and
3) link *n* input terminals to *n* output terminals in any order in *logn* (bit) steps.

The processors and algorithms needed for these operations are extremely simple. For example, in order to sort a list of *n* *m*-bit words, each node need only contain a few *and* and *or* gates. The algorithm for this operation proceeds as follows. Starting at the roots, the *ith* word to be sorted is input (bit by bit) into the *ith* row and column trees for each *i*, $1 \leq i \leq n$. The bits are passed down each tree so that after *logn* steps the leading bit of the *ith* word has reached each leaf of the *ith* row and column trees. Comparison of the *ith* and *jth* words for all *i* and *j* can then proceed simultaneously. After at most *m* additional steps, the (*i,j*) leaf has decided whether the *ith* word is smaller or larger than the *jth* word. Ties are broken arbitrarily (e.g., depending on the values of *i* and *j*). Once this is done, each leaf transmits a *0* or a *1* to its column tree father depending on whether its column tree word was smaller or larger than its row tree word. Each column tree then sums these values in order to determine the position of its word in the final ordering. (If the sum is carried out bit by bit starting with the least significant bit, this process takes *2logn* steps.) This information is then used to mark a path in each column tree from the root to that leaf which is also in the appropriate row tree (again taking *2logn* steps). Once this is done, it is a simple matter to transmit the bits of the *ith* word along the unique path from the *ith* column tree root to the appropriate row root for each *i*. As the paths are all pairwise disjoint, this process takes only *m+2logn* steps.

The algorithm just described sorts a list of *n* *m*-bit numbers in *2m+7logn* steps. It is a simple exercise to speed up the algorithm to obtain the *2m+5logn* step bound. We should also point out that this algorithm is similar to the one described by Muller and Preparata in [MP75]. The VLSI implementation of the algorithm is new, however, and far superior to many of the VLSI sorting algorithms discussed by Thompson in his recent survey paper [T81].

It is easy to show that the nxn mesh of trees has $N=3n^2-2n$ nodes, bisection width $n=\Theta(N^{1/2})$, and an $O(x^{1/2})$-separator. In Theorems 3, 5 and 8 (respectively) we will show that any layout for the N-node 2-dimensional mesh of trees has

1) at least $\Omega(N\log N)$ crossings,
2) at least $\Omega(N\log^2 N)$ wire area, and
3) some edge of length at least $\Omega(N^{1/2}\log N/\log\log N)$.

(It is worth noting that all of these bounds are tight.)

(2b) The r-dimensional Mesh of Trees

The 2-dimensional mesh of trees can be easily generalized to higher dimensions. For example, the *3-dimensional nxnxn mesh of trees* $M_{3,n}$ can be constructed as follows. Starting with an $nxnxn$ cube of nodes and adding nodes wherever necessary, construct a set of n^2 complete binary trees in each of the three dimensions of the cube. As before, the trees should be constructed so that the leaves are precisely the nodes of the original cube and so that the subgraph induced on each octant of nodes is $M_{3,n/2}$.

The $nxnxn$ mesh of trees is also a very useful network for parallel computation. For example, it can be used to compute the products of m pairs of nxn matrices in $m+2\log n$ (word) steps. The algorithm and processors needed for this operation are quite simple. The algorithm proceeds as follows. At each time step, a pair of matrices is entered into the network via the roots of the trees in two of the dimensions (one dimension for each matrix). The entries are passed down through the trees so that after $\log n$ steps, the leaf in the (r,s,t) position of the cube contains the (r,s) entry of the first matrix and the (s,t) entry of the second matrix for each r,s and t. All n^3 multiplications can then be performed simultaneously. The entries of the product matrix are then calculated by summing the values of the leaves of each tree in the third (previously unused) dimension. This process takes an additional $\log n$ steps. As the network is easily pipelined, it is clear that the total computation time is just $m+2\log n$ (word) steps.

A simple counting argument reveals that $M_{3,n}$ has $N=4n^3-2n^2$ nodes for each n and that the class of such graphs has an $O(x^{2/3})$-separator theorem. Thus the N-node 3-dimensional mesh of trees can be laid out in $O(N^{4/3})=O(n^4)$ area. As the the bisection width of the network has size $\Theta(N^{2/3})$, we can conclude that the layout

area is precisely $\Theta(N^{4/3})$. At the same time, we can also observe that the network nearly achieves the optimal AT^2 bound for matrix multiplication [T79]. Although Preparata and Vuillemin [PV80] have already found an optimal network for fast matrix multiplication, it appears that $M_{3,n}$ is much simpler and far easier to program.

Our primary interest in the higher dimensional meshes of trees is not in their computational power, however. We are interested more in the fact that all layouts for such graphs must have very long edges. In fact, we will show in Theorem 4 that any layout for the N-node r-dimensional mesh of trees must have an edge of length $\Theta(N^{1-1/r})$ for any N and $r \geq 3$. It is not difficult to show that the r-dimensional mesh of trees has an $O(x^{1-1/r})$-separator and thus that such edges are (up to a constant) as long as the side length of any optimal layout.

(2c) The Tree of Meshes

The *tree of meshes* is similar to the 2-dimensional mesh of trees in that it combines the structure of a mesh with that of a complete binary tree in a natural way. Unlike the 2-dimensional mesh of trees, however, the tree of meshes is a planar graph. It is formed by replacing each node of a complete binary tree with a mesh and each edge by several edges which link the meshes together. More precisely, the root of the binary tree is replaced by an nxn mesh (where n is assumed to be a power of 2), its sons are replaced by $n/2 \times n$ meshes, their sons are replaced by $n/2 \times n/2$ meshes, and so on until the leaves are replaced by $1x1$ meshes. In the place of each *right edge* of the binary tree (i.e., one which links a node to its right son), we link the rightmost column of nodes in the mesh corresponding to the father to the topmost row of nodes in the mesh corresponding to the right son. Similar replacements are made for *left edges* of the binary tree. In both cases, the connections are made so as to preserve the column and row order of the nodes and to insure that the resulting graph is planar. A simple counting argument reveals that the resulting graph (which we call the nxn tree of meshes T_n) has $N = 2n^2 \log n + n^2$ nodes. For example, we have drawn T_4 in Figure 3.

The tree of meshes is a particularly interesting planar graph since it can embed arbitrary planar graphs much more efficiently than can the ordinary mesh. For example, it is not known how to embed an arbitrary planar graph in less than an $\Theta(N \log^2 N)$-node mesh. As we show in our thesis [L81a], however, any N-node planar graph can be embedded in an $O(N \log N)$-node tree of meshes. Thus the tree

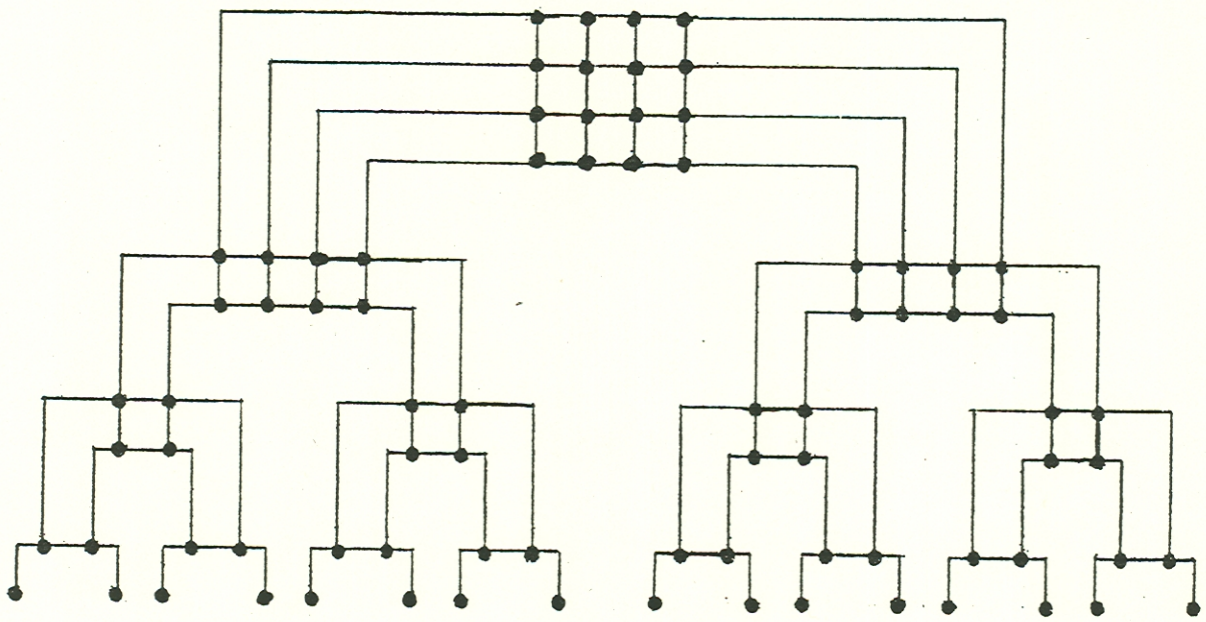

Figure 3: *The 4x4 tree of meshes T_4.*

of meshes is an excellent candidate for a planar graph which cannot be laid out in linear area. In fact, we will show in Theorem 6 that the N-node tree of meshes has layout area $\Omega(N \log N)$.

The tree of meshes can also be used to embed many nonplanar graphs which have $O(x^{1/2})$-separators. Of particular interest here is the fact that $M_{2,n}$ can be embedded in T_{2n} for any n. In order to construct such an embedding, we first embed (recursively) four copies of $M_{2,n/2}$ in four copies of T_n (one in each). Next, we embed the roots of $M_{2,n}$ in the $2n \times 2n$ mesh of T_{2n}. The embedding of $M_{2,n}$ is completed by using the $n \times 2n$ meshes of T_{2n} as switching networks to link the roots of $M_{2,n}$ to its four subgraphs $M_{2,n/2}$ (each of which is already embedded in a copy of T_n).

As an example of the procedure, we have included the embedding of $M_{2,4}$ in T_8 in Figure 4. The embedding has been drawn as though it were constructed as part of a larger embedding (say, of $M_{2,8}$) in order to illustrate the recursive nature of the embedding algorithm. In addition, we have drawn the nodes and edges of $M_{2,4}$ as they appear in Figure 2. For clarity, we have represented the nodes of T_8 as pinpoints and omitted its edges altogether. (For a more complete description of the embedding algorithm, we again refer the reader to [L81a].)

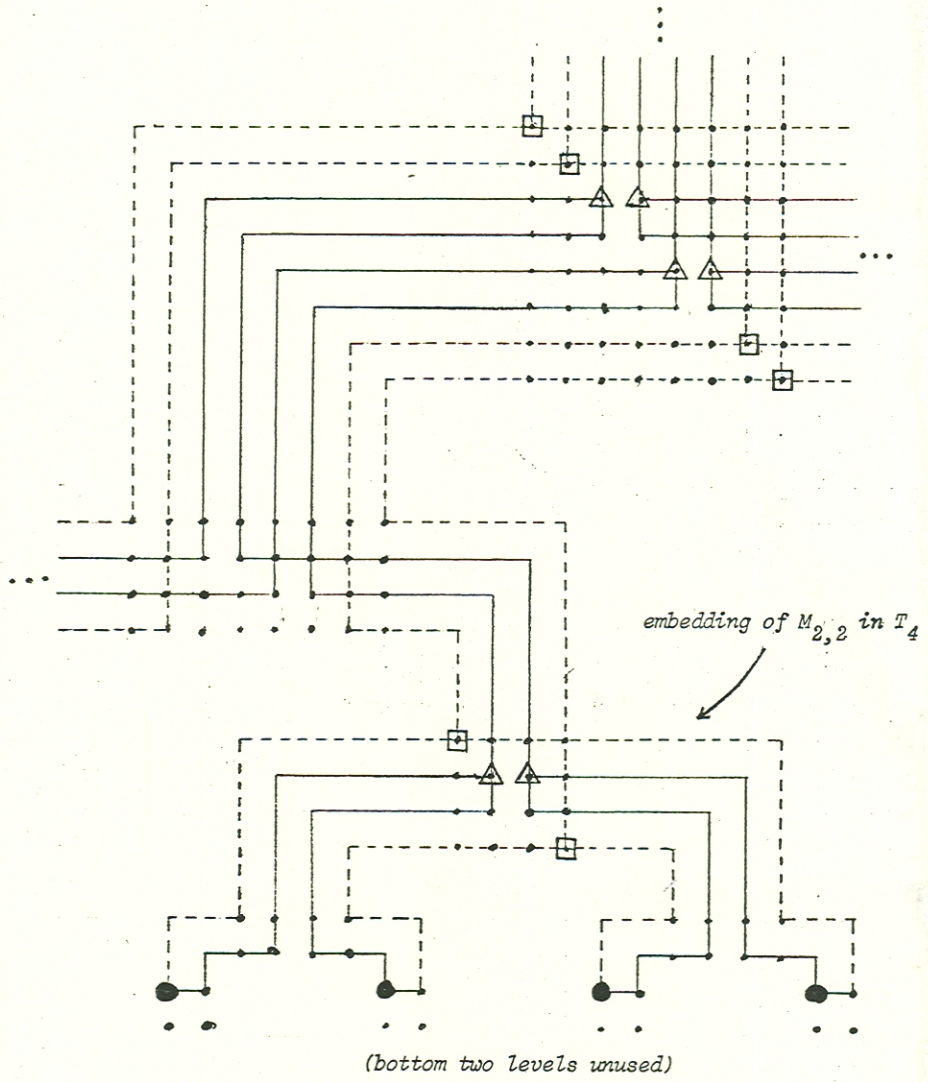

Figure 4: *The embedding of $M_{2,4}$ in T_8.*

As we will show in Theorem 5, any layout for $M_{2,n}$ requires $\Omega(n^2 log^2 n)$ area. Thus it is easy to see that any layout for T_{2n} also requires $\Omega(n^2 log^2 n)$ area. Equivalently, any layout for the N-node tree of meshes requires at least $\Omega(NlogN)$ area. (It is worth noting that an $O(NlogN)$-area layout for the N-node tree of meshes can, in fact, be constructed by expanding the standard H-tree layout for binary trees.)

(2d) The Augmented Tree of Meshes

In [L81a], we show that the maximum edge length of the N-node tree of meshes is $\Theta(logN)$. By slightly modifying the graph, however, it is possible to increase the maximum edge length dramatically. The basic idea is to add a complete binary tree with n^2 leaves to the nxn tree of meshes so that the leaves of one are linked in a one-to-one fashion to the leaves of the other. It is important that the attachments between the two graphs be made so that the resulting graph (which we call the *nxn augmented tree of meshes* T_n') is planar. For example, we have drawn the *4x4* augmented tree of meshes in Figure 5.

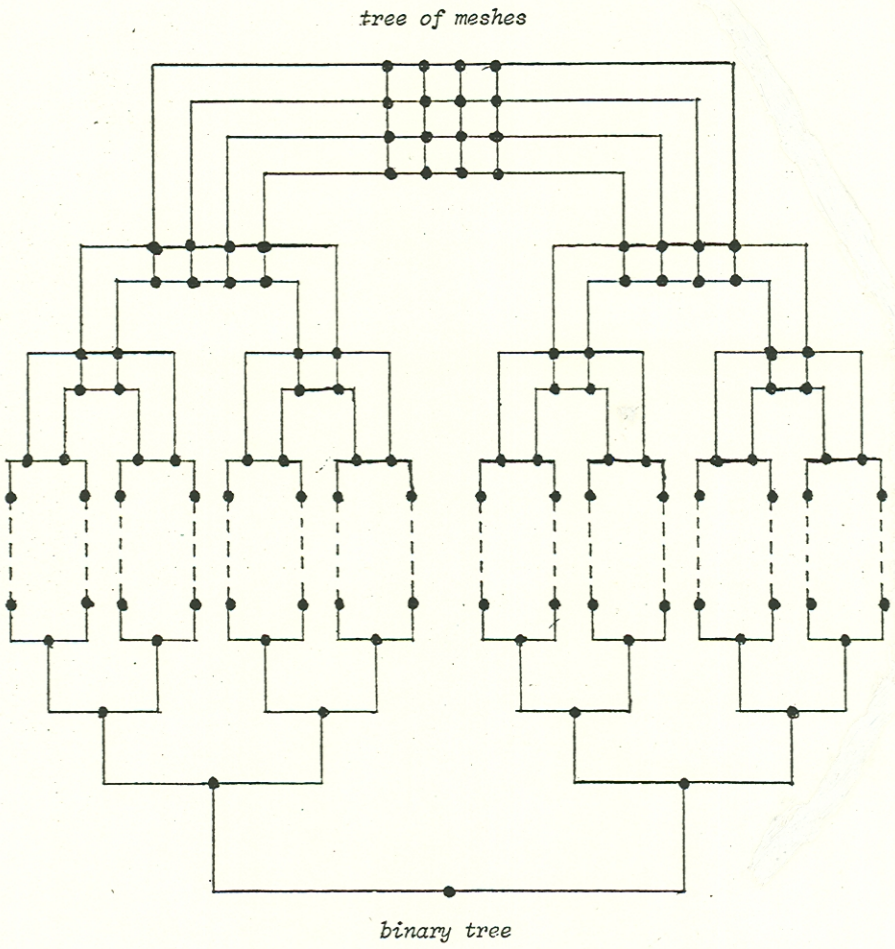

Figure 5: *The 4x4 augmented tree of meshes* T_4'.

It is easily seen that the augmented tree of meshes has, up to a constant, the same bisection width, separator, layout area and number of nodes as does the original tree of meshes. By adding the binary tree, we have simply decreased the *distance* (i.e., the length of the shortest path) between any two *leaves* of the tree of meshes. In section 4, we will show that any layout of the N-node tree of meshes must have two leaves which are spaced at least $\Omega(N^{1/2}log^{1/2}N)$ apart. We will thus be able to conclude that the maximum edge length of the N-node *augmented* tree of meshes is at least $\Omega(N^{1/2}/log^{1/2}N)$. Using arguments similar to those found in [BL81], it can be shown that this bound is tight.

3. Crossing Number Arguments

(3a) General Results

We first demonstrate the power of the crossing number as a general lower bound technique for layout area.

Theorem 1: *If G is an N-node graph with crossing number C and bisection width B, then* $C+N \geq \Omega(B^2)$.

Proof: Let D be a drawing of G in the plane with C crossings. Replace each crossing of D with an *artificial node.* Call the resulting graph G' and note that it has precisely $C+N$ nodes. Using the weighted version of the Lipton-Tarjan planar separator theorem [LT80], it is possible to bisect the real nodes of G' (by assigning weight 1 to the real nodes and weight 0 to the artificial nodes) without cutting more than $O((C+N)^{1/2})$ edges. After replacing the artificial nodes with their original edge crossings, it becomes apparent that we have, in fact, constructed an $O((C+N)^{1/2})$ bisection for G. Squaring, we find that $C+N \geq \Omega(B^2)$ □

Using a similar proof technique, we can show that the crossing number is also close to an *upper* bound for the layout area of a graph. In fact, should a really good layout algorithm for planar graphs be found, then the following result could become useful in laying out arbitrary graphs.

Theorem 2: *Given an optimal drawing D for an N-node graph G with crossing number C, it is possible to construct a layout for G with area at most* $O((C+N)log^2(C+N))$. *Should a procedure be found which lays out an arbitrary*

N-node planar graph in $A(N)$ area, then we could construct a layout for G with area at most $O(A(C+N))$.

Proof: As in the proof of Theorem 1, we replace each edge crossing of D with an artificial node. The resulting graph G' has $C+N$ nodes and is planar. Using the methods developed by Lipton and Tarjan [LT80] and Leiserson [L80a], G' can be laid out in $O((C+N)log^2(C+N))$ area. It is then a simple matter to replace the artificial nodes with their original edge crossings to obtain the desired layout for G. Alternatively, should an $A(N)$-area planar graph layout procedure be discovered, we could construct an $O(A(C+N))$-area layout for G □.

As we have just seen, the idea of replacing edge crossings with artificial nodes is simple but powerful. Jai-Wei and Rosenberg have also employed this strategy in their work with embeddings of graphs in binary trees [JR81].

(3b) Specific Lower Bounds

From Theorem 1, we know that crossing number arguments can give good lower bounds on the layout area of many graphs. For example, we could simply reformulate the techniques developed by Thompson [T79, T80] and others [V80, LS81] in terms of crossing numbers. Of much greater interest, however, is the fact that there are also several purely combinatorial techniques for proving crossing number lower bounds. (For example, see Kleitman's work [K70] and our thesis [L81a].) In what follows, we will develop a new procedure for proving crossing number lower bounds in order to show that the crossing number of the N-node 2-dimensional mesh of trees is at least $\Omega(NlogN)$. We will also show that any drawing of the N-node r-dimensional mesh of trees contains an edge which crosses at least $\Omega(N^{1-1/r})$ other edges.

Our results require the following standard result. For completeness we have included one of the many proofs from [K70].

Lemma 1: *The crossing number of K_N, the complete graph on N nodes, is at least $N(N-1)(N-2)(N-3)/120$ for $N \geq 5$.*

Proof: Let D be a drawing of K_N in the plane with the smallest possible number of crossings $C(N)$. We may assume that no pair of edges which cross in D are incident to a common node. Otherwise, it would be possible to produce a drawing

D' for K_N with $C(N)-1$ crossings by exchanging the parts of the crossing edges which lie between the common node and the point of crossing. This would contradict the minimality of $C(N)$.

Consider the N subdrawings of D obtained by deleting one of the nodes and all of the edges incident to it. Note that each crossing of D appears in precisely $N-4$ of the subdrawings. (A crossing does not appear in any of the 4 subdrawings which correspond to the deletion of a node incident to an edge of the crossing.) Since each of the subdrawings is a drawing of K_{N-1}, each must have at least $C(N-1)$ crossings. Thus $(N-4)C(N) \geq NC(N-1)$. Applying the inequality recursively and noting that $C(5)=1$, we can conclude that

$$C(N) \geq [N/(N-4)]\,[(N-1)/(N-5)]\cdots[6/2]$$

$$= N(N-1)(N-2)(N-3)/120 \quad \text{for } N\geq 5 \quad \square$$

Theorem 3: *The crossing number of the N-node 2-dimensional mesh of trees is at least* $\Omega(N\log N)$.

Proof: As before, let $M_{2,n}$ denote the 2-dimensional mesh of trees (where n is a power of 2). We will show that the crossing number of $M_{2,n}$ is at least

$$(n^2\log n - 121n^2 + 121n)/40 \quad \text{for all } n\geq 1.$$

Since $M_{2,n}$ has $N=\Theta(n^2)$ nodes, this will be sufficient to prove the desired result.

The proof consists of two steps. In the first, we show how to construct a drawing of K_{n^2} from any drawing of $M_{2,n}$ by tracing over the edges of $M_{2,n}$. We then apply Lemma 1 to conclude that there are a large number of crossings among the edges in the top levels of the binary trees of $M_{2,n}$. In the second step, we complete the proof by inductively applying the result of the first step.

step 1: Let D be any drawing of $M_{2,n}$ in the plane. From this drawing, we can construct a drawing D' of K_{n^2} in the following way. First locate the n^2 leaves of the binary trees of D. They will serve as the nodes for K_{n^2}. Given any pair (i,j) and (k,l) of these nodes, draw an edge from (i,j) to (k,l) along the unique path from (i,j) to (i,l) in the ith row tree of D and then from (i,l) to (k,l) in the lth column tree of D. (In order that each edge not be drawn twice, we shall assume that $i\leq k$ and, when $i=k$, that $j<l$.) As edges in D will be traced over several times by this procedure, it is important to draw the edges of D' so that no pair cross each other more than once.

We next count the number of crossings in D'. There are two kinds of crossings to consider. The *first kind* results from a crossing in D. More precisely, if e_1 and e_2 are edges of $M_{2,n}$ which cross in D and e_1 is traced over s_1 times while e_2 is traced over s_2 times, then the crossing of e_1 and e_2 will appear $s_1 s_2$ times in D'. This phenomenon is illustrated in Figure 6.

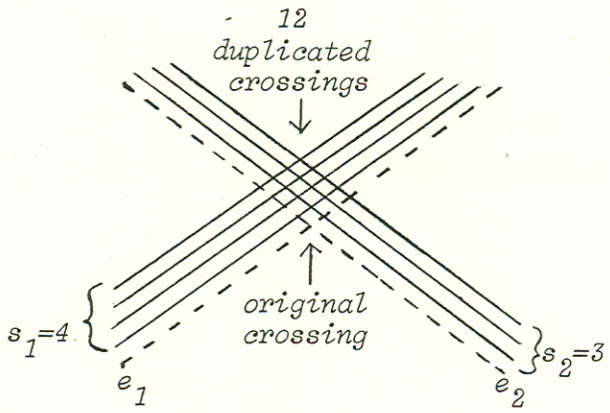

Figure 6: *Crossings of the first kind.*

The *second kind* of crossing results from edges of K_{n^2} which must cross while traversing a common edge of D. For example, see Figure 7. In what follows, we will show that the number of crossings of the second kind is relatively small.

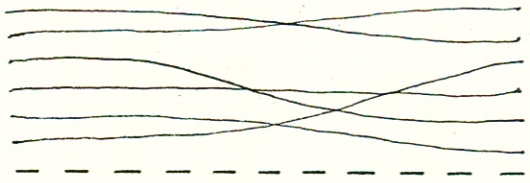

Figure 7: *Crossings of the second kind.*

We say that an edge is *type i* if it is in the *ith* level of a binary tree of $M_{2,n}$. It is not difficult to show that each type i edge is traced over at most

$$n2^{-i}(n^2-n^2 2^{-i}) \leq n^3 2^{-i}$$

times for any $i \leq \log n$ during the construction of D'. Thus at most $n^6 2^{-2i-1}$ crosses of the second kind can occur at any type i edge of D. Since there are $2^{i+1}n$ type i edges in $M_{2,n}$, we can conclude that the total number of crosses of the second kind in D' is at most

$$\sum_{i=1}^{\log n}(2^{i+1}n)(n^6 2^{-2i-1}) = n^7 \sum_{i=1}^{\log n} 2^{-i} \leq n^7.$$

We next count the number of crossings of the first kind (i.e., those corresponding to crosses in D). We say that a crossing of D is *type i-j* if it is the crossing of a type i edge and a type j edge. Let t_{ij} denote the number of type i-j crossings in D and set

$$t_i = \sum_{j=i}^{\log n} t_{ij} .$$

Since each type i edge is traced over at most $n^3 2^{-i}$ times, each type i-j crossing of D produces at most

$$(n^3 2^{-i})(n^3 2^{-j}) = n^6 2^{-i-j}$$

crosses of the first kind in D'. Thus the total number of crossings of the first kind in D' is at most

$$\sum_{i=1}^{\log n}\sum_{j=i}^{\log n} n^6 2^{-i-j} t_{ij} \leq n^6 \sum_{i=1}^{\log n} 2^{-2i} t_i .$$

Summing, we find that the total number of crossings of either kind in D' is at most

$$n^7 + n^6 \sum_{i=1}^{\log n} 2^{-2i} t_i .$$

By Lemma 1, this number must be at least

$$n^2(n^2-1)(n^2-2)(n^2-3)/120 \quad \text{for} \quad n^2 \geq 5.$$

Simplifying, we can conclude that

$$\sum_{i=1}^{\log n} 2^{-2i} t_i \geq (n^2-121n)/120 \quad \text{for } n \geq 6.$$

Let $s_k = \sum_{i=1}^{k} t_i$ be the number of crossings involving at least one edge from the top k levels of some binary tree of $M_{2,n}$. In what follows, we will use the preceding inequality to show that $s_k \geq (n^2-121n)k/40$ for at least one value of $k \geq 1$. Assume otherwise and observe that

$$\sum_{i=1}^{\log n} 2^{-2i} t_i \;=\; \sum_{i=1}^{\log n} 2^{-2i}(s_i - s_{i-1})$$

where s_0 is defined to be 0. The coefficient of each s_i in this sum is positive so for each i we may substitute $(n^2-121n)i/40$ as an upper bound for s_i in order to see that

$$\sum_{i=1}^{\log n} 2^{-2i} t_i \;<\; [(n^2-121n)/40] \sum_{i=1}^{\log n} 2^{-2i}[i-(i-1)]$$

$$= [(n^2-121n)/40] \sum_{i=1}^{\log n} 4^{-i} \;.$$

Since $\sum_{i=1}^{\log n} 4^{-i} \le 1/3$ for all n, we can conclude that

$$\sum_{i=1}^{\log n} 2^{-2i} t_i \;<\; (n^2-121n)/120$$

for all $n>121$, a contradiction. Thus for all $n>121$, there is a $k\ge 1$ such that

$$s_k \ge (n^2-121n)k/40.$$

step 2: Let $C(n)$ denote the crossing number of $M_{2,n}$. Using the result of step 1, we will now show by induction on n that $C(n) \ge (n^2 \log n - 121n^2 + 121n)/40$ for all $n \ge 1$.

As $(n^2 \log n - 121n^2 + 121n)/40$ is nonpositive for small n, the lower bound trivially holds for all $n<128$. Assume that the lower bound holds for all $m<n$ where $n \ge 128$ and let D be any drawing for $M_{2,n}$. By counting the crossings of D in two groups according to whether or not at least one edge of the crossing is contained in the top k levels of the binary trees of $M_{2,n}$, we can observe that

$$C(n) \;\ge\; 2^{2k} C(n2^{-k}) + s_k .$$

(Recall the definition of s_k and the structure of $M_{2,n}$.) By choosing k as in step 1 so that $s_k \ge (n^2-121n)k/40$ and applying the inductive hypothesis for $C(n2^{-k})$, we obtain

$$C(n) \;\ge\; 2^{2k}[n^2 2^{-2k}(\log n - k)/40 - 121n^2 2^{-2k}/40 + 121n2^{-k}/40] + n^2k/40 - 121nk/40$$

$$\ge\; n^2 \log n/40 - 121n^2/40 + 121n/40 + 121n(2^k - k - 1)/40$$

$$\ge\; (n^2 \log n - 121n^2 + 121n)/40 \;.$$

Thus the inductive hypothesis is established and we can conclude that the crossing number of $M_{2,n}$ is at least $\Omega(n^2 \log n) = \Omega(N \log N)$ □

Theorem 4: *Any drawing of the N-node r-dimensional mesh of trees contains an edge which crosses at least* $\Omega(N^{1-1/r})$ *other edges.*

Proof: The r-dimensional $nxnx\cdots xn$ mesh of trees $M_{r,n}$ has $N = (r+1)n^r - rn^{r-1} = \Theta(n^r)$ nodes for bounded r. We will show that any drawing D of $M_{r,n}$ contains an edge which crosses at least $\Omega(n^{r-1}) = \Omega(N^{1-1/r})$ other edges, thus proving the theorem. The method used is very similar to that of Theorem 3.

As we did for the case of $r=2$ in Theorem 3, we first construct a drawing D' of the complete graph on the n^r leaves of $M_{r,n}$. Each type i edge of D is traced over at most $n^{r+1}2^{-i}$ times by this procedure. Thus the total number of crossings in D' is at most

$$(rn^{3r+1})/2 \quad + \quad n^{2r+2}\sum_{i=1}^{\log n} 2^{-2i}t_i$$

where, as before, $t_i = \sum_{j=i}^{\log n} t_{ij}$ and t_{ij} is the number of type i-j crossings in D. Applying Lemma 1, we can conclude that

$$\sum_{i=1}^{\log n} 2^{-2i}t_i \quad \geq \quad \Omega(n^{2r-2}).$$

Let $s_k = \sum_{i=1}^{k} t_i$ be the total number of crossings of D involving an edge from the top k levels of the binary trees in $M_{r,n}$. Using arguments similar to those used to prove Theorem 3, it is not difficult to show that for large n, there exists a k such that $s_k \geq \Omega(n^{2r-2}2^k)$. As there are only $rn^{r-1}(2^{k+1}-2)$ edges in the top k levels of $M_{r,n}$ for any k, we can conclude that at least one of them crosses at least $\Omega(n^{r-1})$ other edges □

4. Wire Area Arguments

As we have just seen, crossing number arguments can be very powerful in establishing lower bounds on layout area and maximum edge length for VLSI networks. Such arguments are also limited, however, to the kinds of results obtained in the previous section. For example, in our thesis [L81a], we show that the crossing number of any N-node graph with an $O(x^{1/2})$-separator is at most $O(N\log N)$. Thus, we could not hope to improve the result of Theorem 3. Nor can crossing number arguments be used to prove any nontrivial lower bounds for planar graphs.

The technique of using a drawing of a network to construct a drawing for the

complete graph *can* be extended, however. In what follows, we use this technique to find better lower bounds on the wire area of certain networks than were possible with crossing number arguments alone. More precisely, we will show that the wire area of the N-node 2-dimensional mesh of trees is at least $\Omega(N\log^2 N)$ and, as a corollary, that the N-node (planar) tree of meshes has wire area at least $\Omega(N\log N)$. In addition, we will show that the maximum edge length of the N-node 2-dimensional mesh of trees is at least $\Omega(N^{1/2}\log N/\log\log N)$ while that of the N-node augmented tree of meshes is at least $\Omega(N^{1/2}/\log^{1/2} N)$.

Theorem 5: *The wire area of the N-node 2-dimensional mesh of trees is at least* $\Omega(N\log^2 N)$.

Proof: As usual, we denote the nxn mesh of trees by $M_{2,n}$. In addition, let $W(n)$ denote the wire area of $M_{2,n}$ and let α be a positive constant such that

(*) $\alpha \leq n/(4\log^2 n)$ for all $n \geq 2$, and

(**) $\alpha \leq 2^{2i-20}/(\beta^2 i^6)$ for all $i \geq 1$ where $\beta = \sum_{j=1}^{\infty} j^{-2}$ is also a constant.

Clearly such a constant exists ($\alpha = 2^{-30}$ should suffice) and clearly $W(n) \geq \alpha n^2 \log^2 n$ for $n = 1$ and 2. Consider a value of $n \geq 4$ which is a power of 2 and assume that for all values of $m < n$ which are powers 2 that $W(m) \geq \alpha m^2 \log^2 m$. We will use induction to show that $W(n) \geq \alpha n^2 \log^2 n$. Since $M_{2,n}$ has $N = \Theta(n^2)$ nodes, this will be sufficient to prove the theorem.

Consider any layout for $M_{2,n}$ which uses $W(n)$ wire. Partition the layout into three vertical strips V_0, V_1 and V_2 so that the center strip contains $3n^2/4$ leaves and each outer strip contains $n^2/8$ leaves. Similarly partition the layout into three horizontal strips H_0, H_1 and H_2 so that the middle strip contains $3n^2/4$ leaves and each outer strip contains $n^2/8$ leaves. For example, see Figure 8.

Let d denote the length of the longest side of the center block formed by the intersection of V_1 and H_1. Without loss of generality, we assume that the longest side is horizontal. In what follows, we will show that $d \geq (\alpha^{1/2} n \log n)/8$.

Since each of the regions $V_0 \cap H_1$ and $V_2 \cap H_1$ can contain at most $n^2/8$ leaves, it is clear that $V_1 \cap H_1$ contains at least $n^2/2$ leaves. Consider the $n^{3/2}$ subgraphs of $M_{2,n}$ produced by eliminating the top $(3\log n)/4$ levels of the row and column binary trees of $M_{2,n}$. Each of these subgraphs is isomorphic to $M_{2,n^{1/4}}$. By the

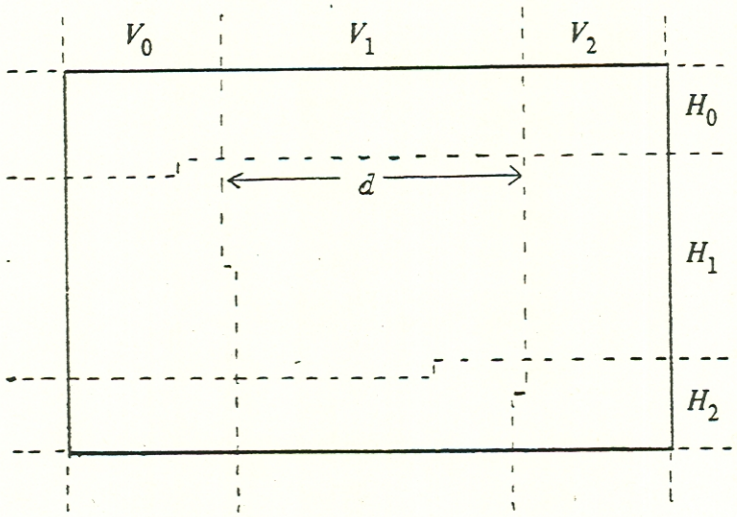

Figure 8: *Partitioning of the layout for* $M_{2,n}$.

pigeonhole principle, at least $1/2$ of these subgraphs have at least one leaf in $V_1 \cap H_1$. If $d < (\alpha^{1/2} n \log n)/8$ (otherwise we are done), then at most $4d < (\alpha^{1/2} n \log n)/2$ edges can cross the boundary of $V_1 \cap H_1$. Thus at most $(\alpha^{1/2} n \log n)/2$ of the subgraphs which have at least one leaf in $V_1 \cap H_1$ can also have a node or part of an edge outside $V_1 \cap H_1$. This means that at least $(n^{3/2} - \alpha^{1/2} n \log n)/2$ copies of $M_{2,n^{1/4}}$ are wholly contained in $V_1 \cap H_1$. Applying the inductive hypothesis, we conclude that $V_1 \cap H_1$ contains at least

$$(n^{3/2} - \alpha^{1/2} n \log n)\, W(n^{1/4}) / 2 \geq (\alpha n^2 \log^2 n - \alpha^{3/2} n^{3/2} \log^3 n) / 32$$

$$\geq (\alpha n^2 \log^2 n)/64 \quad \text{wire.}$$

The last inequality follows trivially from (*). Thus $V_1 \cap H_1$ has at least $(\alpha n^2 \log^2 n)/64$ area and $d \geq (\alpha^{1/2} n \log n)/8$, as claimed.

We next use the (Thompson model) layout for $M_{2,n}$ to construct a drawing for the complete graph on n^2 nodes (namely, the n^2 leaves of $M_{2,n}$). No matter how the edges of the complete graph are drawn in the plane (e.g., they may cross or overlap), it is clear from Figure 8 that the sum of the lengths of all the edges (as measured in Euclidean space) is at least $n^4 d/64 \geq (\alpha^{1/2} n^5 \log n)/2^9$. This is due to the fact that $n^4/64$ edges pass from region V_0 to region V_2 and that these regions are separated by a distance d.

Let L_i denote the sum of the lengths of the edges in the ith levels of the binary trees of $M_{2,n}$. Since every level i edge is traced over at most $n^3 2^{-i}$ times in the

drawing of the complete graph, we can conclude that

$$\sum_{i=1}^{\log n} L_i 2^{-i} n^3 \geq (\alpha^{1/2} n^5 \log n)/2^9$$

and thus that

$$\sum_{i=1}^{\log n} L_i 2^{-i} \geq (\alpha^{1/2} n^2 \log n)/2^9 .$$

In particular, this means that

$$L_i \geq (\alpha^{1/2} n^2 \log n 2^i)/(2^9 \beta i^2)$$

for some $i < \log n$. (Recall that $\beta = \sum_{j=1}^{\infty} j^{-2}$.) Otherwise,

$$L_i < (\alpha^{1/2} n^2 \log n 2^i)/(2^9 \beta i^2)$$

for $1 \leq i \leq \log n$ and thus

$$\sum_{i=1}^{\log n} L_i 2^{-i} < \sum_{i=1}^{\log n} (\alpha^{1/2} n^2 \log n)/(2^9 \beta i^2)$$
$$\leq (\alpha^{1/2} n^2 \log n)/2^9, \quad \text{a contradiction.}$$

Using the straightforward relation

$$W(n) \geq 2^{2i} W(n2^{-i}) + L_i$$

where i has been chosen so that

$$L_i \geq (\alpha^{1/2} n^2 \log n 2^i)/(2^9 \beta i^2),$$

we can conclude that

$$W(n) \geq 2^{2i} \alpha (n2^{-i})^2 (\log n - i)^2 + (\alpha^{1/2} n^2 \log n 2^i)/(2^9 \beta i^2)$$
$$\geq \alpha n^2 \log^2 n - 2\alpha i n^2 \log n + (\alpha^{1/2} n^2 \log n 2^i)/(2^9 \beta i^2)$$
$$\geq \alpha n^2 \log^2 n .$$

The last inequality follows trivially from (**). Thus $W(n) \geq \Omega(n^2 \log^2 n)$ for all n □

Theorem 6: *The wire area of the N-node tree of meshes is at least* $\Omega(N \log N)$.

Proof: As we showed in section 2c of this paper, the N-node 2-dimensional mesh of trees can be embedded in an $O(N \log N)$-node tree of meshes. From Theorem 5, we can thus conclude that the wire area of the $(N \log N)$-node tree of meshes is at

least $\Omega(N\log^2 N)$. Equivalently, the wire area of the N-node tree of meshes is at least $\Omega(N\log N)$ □

Theorem 7: *Any layout of the N-node augmented tree of meshes contains a wire of length at least* $\Omega(N^{1/2}/\log^{1/2} N)$.

Proof: In the proof of Theorem 5, we showed that any layout of $M_{2,n}$ must have two leaves which are spaced at least $\Omega(n\log n)$ distance apart. Since $M_{2,n}$ can be embedded in T_{2n} so that the leaves of $M_{2,n}$ are embedded in or near the leaves of T_{2n} (see the embedding in section 2c), we can observe that any layout of T_{2n} must also have two leaves which are spaced at least $\Omega(n\log n)$ distance apart. Since any pair of leaves in T_{2n} are linked by a path of length at most $O(\log n)$ in T_{2n}', we can conclude that some edge of T_{2n}' must have length at least $\Omega(n)=\Omega(N^{1/2}/\log^{1/2} N)$ □

It is worthwhile to point out that we could have proved both Theorems 6 and 7 directly, using arguments similar to the ones used to prove Theorem 5.

Theorem 8: *Any layout of the N-node 2-dimensional mesh of trees contains a wire of length at least* $\Omega(N^{1/2}\log N/\log\log N)$.

Proof: It is sufficient to show that any layout for $M_{2,n}$ contains a wire of length at least $\Omega(n\log n/\log\log n)$. Assume for the purposes of contradiction that this is *not* the case and consider a layout of $M_{2,n}$ for which the longest wire has length $q \leq o(n\log n/\log\log n)$. We first show that (without loss of generality) the area of such a layout is at most $O(q^2\log^2 n) \leq o(n^2\log^4 n)$.

Since every pair of nodes of $M_{2,n}$ is linked by a path of length at most $4\log n$, all of the nodes in the layout are contained in a $4q\log n \times 4q\log n$ square. At most $16q\log n$ wires may leave and re-enter the square at various points along its perimeter. Without increasing the lengths of any of these wires, it is possible to rewire the segments outside the square using at most $O(q^2\log^2 n)$ additional area. Thus, the resulting layout for $M_{2,n}$ will have maximum edge length q and area at most $O(q^2\log^2 n)$.

The proof is completed by observing that any layout of $M_{2,n}$ with area $o(n^2\log^4 n)$ must have a wire of length at least $\Omega(n\log n/\log\log n)$. From the proof of Theorem 5, we know that

$$\sum_{i=1}^{\log n} L_i 2^{-i} \geq (\alpha^{1/2} n^2 \log n)/2^9 .$$

Thus either

1) there is an $i \leq 4loglogn$ such that

$$L_i \geq (\alpha^{1/2} n^2 logn 2^i) / (2^{12} loglogn),$$ or

2) there is an $i > 4loglogn$ such that

$$L_i \geq (\alpha^{1/2} n^2 logn 2^i) / (2^{10} \beta i^2)$$

where, as before, the constant $\beta = \sum_{j=1}^{\infty} j^{-2}$. Otherwise,

$$\sum_{i=1}^{logn} L_i 2^{-i} = \sum_{i=1}^{4 loglogn} L_i 2^{-i} + \sum_{i=4loglogn+1}^{logn} L_i 2^{-i}$$

$$< (\alpha^{1/2} n^2 logn)/2^{10} + [(\alpha^{1/2} n^2 logn)/2^{10}\beta] \sum_{i=1}^{\infty} i^{-2}$$

$$\leq (\alpha^{1/2} n^2 logn)/2^9 , \quad \text{a contradiction.}$$

The second condition cannot possibly be true, however. If it were, the area of the layout would be at least $L_i \geq \Omega(n^2 logn 2^i / i^2)$ which, for $i > 4loglogn$, means that

$$A \geq \Omega(n^2 log^5 n / (loglogn)^2)$$

$$> \Omega(n^2 log^4 n), \text{ a contradiction.}$$

Thus the *first* condition must be true and there is an i such that $L_i \geq \Omega(n^2 logn 2^i / loglogn)$. Since there are $n2^{i+1}$ type i edges in $M_{2,n}$, we can conclude that at least one of them has length at least $\Omega(nlogn/loglogn)$ □

5. Remarks

(a) In addition to being good lower bounds for layout area, the crossing number and wire area of a network are interesting in their own right. In particular, both are worth minimizing when designing a chip. For instance, a chip with a large number of crossings may have problems with *capacitive coupling* (i.e., interference between overlapping wires); particularly if some of the wires cross an unusually large number of the other wires (as was the case with the r-dimensional mesh of trees). The wire area is worth minimizing in order to maximize the chip yield. As many chips are ruined by localized random errors, chips with lower wire density will be less likely to be affected by such problems.

(b) Unfortunately, our results indicate that both the crossing number and the wire area are usually as large (up to a constant) as the area of the layout. In fact, all of the previously known nontrivial lower bounds for layout area are also lower bounds for crossing number and wire area. This is due to the fact that the previously known lower bounds for layout area were proved as a consequence of the identity $A \geq \Omega(B^2)$. Since we showed in Theorem 1 that $C+N \geq \Omega(B^2)$, the same bounds also hold for crossing number and wire area. For example, this means that any layout of a network which computes an N-point Fourier transform in T steps must have $\Omega(N^2/T^2)$ wire crossings. Hence, we could thus conclude that the N-node shuffle exchange graph and the N-node cube-connected-cycles graph have crossing number $\Omega(N^2/log^2N)$.

(c) The previous analysis can often be carried one step further in order to show that some wires in a layout must cross many other wires. For example, any network which computes an N-point Fourier transform in T steps must have a wire which crosses $\Omega(N/T^2)$ other wires. This is because the network contains $O(N)$ wires but has at least $\Omega(N^2/T^2)$ crossings. In particular, this means that any layout of the N-node shuffle-exchange graph or the N-node cube-connected cycles graph contains a wire which crosses $\Omega(N/log^2N)$ other wires.

(d) The techniques developed in this paper can also be used to reprove other results in the literature. For example, Brent and Kung showed in [BK80] that any layout of the complete N-node binary tree in which the leaves are contained on the boundary of some convex region requires at least $\Omega(NlogN)$ wire area. Subsequently Patterson, Ruzzo and Snyder [PRS81] showed that any such layout with area A must have some wire of length $\Omega(N/log(A/N))$. As we show in [L81a], both of these results can be simply proved using the techniques used to prove Theorems 5 and 8.

(e) The methods which we have used to prove crossing number and wire area lower bounds can also be used to prove bisection width lower bounds. For example, these techniques can be easily used to show that the bisection width of the N-node shuffle-exchange graph is at least $\Omega(N/logN)$ [L81a]. In this case the construction of the complete graph from the drawing of the shuffle-exchange graph bears a strong resemblance to Thompson's [T80] information flow arguments. In fact, it appears that many of Thompson's lower bounds can be reproved in this fashion.

(f) When defining the *2*-dimensional mesh of trees in section 2a, we required that the binary trees be constructed so that $M_{2,n}$ contain 2^{2k} disjoint copies of $M_{2,n2^{-k}}$ as subgraphs for any k. It is interesting to note that networks which do not satisfy this constraint but which are similar to the *2*-dimensional mesh of trees in all other respects have essentially the same computational power as the more restricted mesh of trees. Theorems 3, 5 and 8 do not necessarily apply to such networks, however. In fact, we do not know if the same wire area lower bound need still apply. Using a somewhat different method, however, we have shown in [L81a] that any such network must still have a large crossing number. As a key step in the proof, we generalize Lemma 1 to show that any N-node graph with E edges has crossing number at least $\Omega(E^3/N^2)$ whenever $E \geq 4N$.

(g) The area required to lay out the r-dimensional mesh of trees is very close to that required to lay out the standard mesh of the same size. For example, for $r>2$ the amount of area required for the mesh of trees, $\Theta(n^r)$, is at most a constant times as large as the area required for the standard r-dimensional mesh. Thus the computational power of the standard mesh can be greatly enhanced at little or no cost in layout area by adding the edges of the mesh of trees.

(h) The r-dimensional mesh of trees was defined as a natural generalization of the computationally powerful *2*-dimensional mesh of trees. $M_{r,n}$ can also be viewed as a generalization of the r-cube, also a very powerful communications network. (For example, $M_{r,2}$ is an r-cube with every edge replaced by a path of length *2*.) Viewed in this light, the r-dimensional mesh of trees motivates the definition of a *shuffle-tree graph* in the same way that the r-cube motivates the definition of the shuffle-exchange graph. We would be interested to know if there any practical applications of such a general comunications network.

(i) Using standard techniques, it is not difficult to show that all of the asymptotic lower bounds proved in Theorems 3-8 are tight (although it is likely that the leading constants can be substantially improved). In addition, the drawings and layouts which achieve the lower bounds for crossing number and wire area also achieve the lower bounds for maximal edge crossing and edge length. Thus there are no *area/edge length* tradeoffs for these networks.

(j) After writing the initial version of this paper, we became aware of several other papers which describe parallel computation algorithms using the mesh of trees.

For example:

1) Nath, Maheshwari and Bhatt [NMB81] have used the network (which they call the *orthogonal trees network*) for sorting, discrete Fourier transform, minimum spanning tree, and connected components (as well as many other) problems,
2) Cappello and Steiglitz [CS81] have used the network (which they call the *orthogonal forests*) for integer multiplication, and
3) Gannon [G81] has used the network to find approximate solutions to systems of partial differential equations.

(k) Subsequent to the final writing of this paper, a great deal more was discovered about upper and lower bounds for layout area and crossing number. As a forward pointer, we refer the interested reader to [L82]. Interestingly, no further progress has been made on the planar layout problem.

6. Acknowledgements

In acknowledgement, I would like to thank the following people for their helpful remarks and suggestions: Sandeep Bhatt, Paris Kanellakis, Daniel Kleitman, Dennis Gannon, Charles Leiserson, Margaret Lepley, Gary Miller, Ron Rivest, Arnie Rosenberg and Jim Shearer. I would especially like to thank Gary Miller for his substantial assistance with this work.

A preliminary version of this paper was presented at the 22nd Annual IEEE Symposium on Foundations of Computer Science [L81b].

7. References

[B81] G. M. Baudet, "On the area required by VLSI circuits," *Proceedings of the CMU Conference on VLSI Systems and Computations*, Edited by H. T. Kung, B. Sproull and G. Steele, Computer Science Press, Rockville, Maryland, October 1981, pp. 100-107.

[BK80] R. P. Brent and H. T. Kung, "On the area of binary tree layouts," *Information Processing Letters*, No. 11, 1980, pp. 44-46.

[BL81] S. N. Bhatt and C. E. Leiserson, "Minimizing the longest edge in a VLSI layout," unpublished manuscript, MIT Lab for Computer Science, 1981.

[BPP81] G. Bilardi, M. Pracchi and F. P. Preparata, "A critique and appraisal of VLSI models of computation," *Proceedings of the CMU Conference on VLSI Systems and Computations*, Edited by H. T. Kung, B. Sproull and G. Steele, Computer Science Press, Rockville, Maryland, October 1981, pp. 81-88.

[CM81] B. Chazelle and L. Monier, "A model of computation for VLSI with related complexity results," *Proceedings of the 13th Annual ACM Symposium on Theory of Computation*, May 1981, pp. 318-325.

[CS81] P. R. Cappello and K. Steiglitz, "Area-efficient VLSI structures for multiplying at clock rate," Technical Report #289, Department of EECS, Princeton University, September 1981.

[G81] D. Gannon, personal communication, November 1981.

[JR81] H. Jai-Wei and A. L. Rosenberg, "Graphs that are similar to binary trees," *Proccedings of the 13th Annual ACM Symposium on Theory of Computation*, May 1981, pp. 334-341.

[K70] D. J. Kleitman, "The crossing number of $K_{5,n}$," *Journal of Combinatorial Theory*, Vol. 9, No. 4, December 1970, pp. 315-323.

[KLLM81] D. Kleitman, F. T. Leighton, M. Lepley and G. L. Miller, "New layouts for the shuffle-exchange graph," *Proceedings of the 13th ACM Symposium on Theory of Computing*, May 1981, pp. 278-292.

[L80a] C. E. Leiserson, "Area-efficient graph layouts (for VLSI)," *Proceedings of the 21st Annual IEEE Symposium on Foundations of Computer Science*, October 1980, pp. 270-281.

[L80b] C. E. Leiserson, *Area Efficient VLSI Computation*, Ph.D. dissertation, Department of Computer Science, Carnegie-Mellon University, 1980.

[L81a] F. T. Leighton, *Layouts for the Shuffle-Exchange Graph and Lower Bound Techniques for VLSI*, Ph.D. dissertation, Mathematics Department, Massachusetts Institute of Technology, August 1981. (Also to appear as an MIT Lab for Computer Science Technical Report.)

[L81b] F. T. Leighton, "New lower bound techniques for VLSI," *Proceedings of the 22nd Annual IEEE Symposium on Foundations of Computer Science*, October 1981, pp. 1-12.

[L82] F. T. Leighton, "A layout strategy for VLSI which is provably good," *Proceedings of the 14th Annual ACM Symposium on Theory of Computing*, May 1982, pp. 85-98.

[LM81] F. T. Leighton and G. L. Miller, "Optimal layouts for small shuffle-exchange graphs," *Proceedings of the VLSI 81 Conference*, Edited by J. P. Gray, Academic Press, London, August 1981, pp. 289-299.

[LR82] F. T. Leighton and A. L. Rosenberg, "Three-dimensional circuit layouts," unpublished manuscript, 1982.

[LS81] R. J. Lipton and R. Sedgewick, "Lower bounds for VLSI," *Proceedings of the 13th Annual ACM Symposium on Theory of Computing*, May 1981, pp. 300-307.

[LT80] R. J. Lipton and R. E. Tarjan, "Applications of a planar separator theorem," *SIAM Journal of Computing*, Vol. 9, No. 3, August 1980, pp. 615-627.

[MC80] C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley Publishing Company, Reading, Massachusetts, October 1980.

[MP75] D. E. Muller and F. P. Preparata, "Bounds to complexities of networks for sorting and for switching," *Journal of the ACM*, Vol. 22, No. 2, April 1975, pp. 195-201.

[NMB81] D. Nath, S. N. Maheshwari and P. C. P. Bhatt, "Efficient VLSI networks for parallel processing based on orthogonal trees," unpublished manuscript, 1981.

[PRS81] M. S. Patterson, W. L. Ruzzo and L. Snyder, "Bounds on minimax edge length for complete binary trees," *Proceedings of the 13th Annual ACM Symposium on Theory of Computing*, May 1981, pp. 293-299.

[PV79] F. P. Preparata and J. E. Vuillemin, "The cube-connected-cycles: a versatile network for parallel computation," *Proceedings of the 20th Annual IEEE Symposium on Foundations of Computer Science*, October 1979, pp. 140-147.

[PV80] F. P. Preparata and J. E. Vuillemin, "Area-time optimal VLSI networks for matrix multiplication," *Proceedings of the 14th Princeton Conference on Information Science and Systems*, 1980.

[RS81] W. L. Ruzzo and L. Snyder, "Minimum edge length planar embeddings of trees," *Proceedings of the CMU Conference on VLSI Systems and Computations*, Edited by H. T. Kung, B. Sproull and G. Steele, Computer Science Press, Rockville, Maryland, October 1981, pp. 119-123.

[S79] J. E. Savage, "Area-time tradeoffs for matrix multiplication and related problems in VLSI models," *Proceedings of the 17th Annual Allerton Conference on Communications, Control and Computing*, October 1979, pp. 670-676.

[T79] C. D. Thompson, "Area-time complexity for VLSI," *Proceedings of the 11th Annual ACM Symposium on Theory of Computing*, May 1979, pp. 81-88.

[T80] C. D. Thompson, *A Complexity Theory for VLSI*, Ph.D. dissertation, Department of Computer Science, Carnegie-Mellon University, 1980.

[T81] C. D. Thompson, "The VLSI complexity of sorting," unpublished notes, Computer Science Department, University of California at Berkely, 1981.

[V80] J. E. Vuillemin, "A combinatorial limit to the computing power of VLSI circuits," *Proceedings of the 21st Annual IEEE Symposium on Foundations of Computer Science*, November 1980, pp. 294-300.

[V81] L. G. Valiant, "Universality considerations in VLSI circuits," *IEEE Transactions on Computers*, Vol. C-30, No. 2, February 1981, pp. 135-140.